**M.Tech. (Microelectronics & VLSI Design)**

**Scheme of Evaluation and Syllabi**

**(I to IV Semesters) w.e.f. 2016- 17**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Course** | **Name of the Subject** | **Hours/**  **Week**  **Credit** | | **Internal Assessment Marks** | **Exam/**  **Practical**  **Marks** | **Total**  **Credits** |
| **L** | **P** |
| **I Semester** | | | | | |  |
| **MMVD 101** | **Process Technology for ULSI –I** | **4** | **0** | **40** | **60** | **4** |
| **MMVD 102** | **MOSFET Physics and Sub-Micron Device Modeling** | **4** | **0** | **40** | **60** | **4** |
| **MMVD 103** | **VLSI Design** | **4** | **0** | **40** | **60** | **4** |
| **MMVD 104** | **Digital Signal Processing** | **4** | **0** | **40** | **60** | **4** |
| **MMVD 105** | **Lab Work – I** | **0** | **8** | **40** | **60** | **8** |
|  |  |  | | **200** | **300** |  |
|  |  | **Total** | | **500** | | **24** |
|  | | | | | | |
| **II Semester** | | | | | |  |
| **MMVD 201** | **Process Technology for ULSI –II** | **4** | **0** | **40** | **60** | **4** |
| **MMVD 202** | **Embedded System Design using 8051** | **4** | **0** | **40** | **60** | **4** |
| **MMVD 203** | **Analog CMOS Integrated Circuits** | **4** | **0** | **40** | **60** | **4** |
| **MMVD 204** | **Verilog - Hardware Description Language** | **4** | **0** | **40** | **60** | **4** |
| **MMVD 205** | **Lab Work – II** | **0** | **8** | **40** | **60** | **8** |
|  |  |  | | **200** | **300** |  |
|  |  | **Total** | | **500** | | **24** |
|  | | | | | | |
| **III Semester** | | | | | |  |
| **MMVD 301** | **Program Elective-I\*** | **4** | **0** | **40** | **60** | **4** |
| **MMVD 302** | **Program Electives-I\*** | **4** | **0** | **40** | **60** | **4** |
| **MMVD 303** | **Program Electives-I\*** | **4** | **0** | **40** | **60** | **4** |
| **MMVD 304** | **Minor Project\*\*** | **0** | **8** | **0** | **100** | **8** |
|  |  |  | | **120** | **280** |  |
|  |  | **Total** | | **400** | | **20** |
|  | | | | | | |
| **IV Semester** | | | | | | |
| **MMVD 401** | **Project Dissertation - Evaluation & Viva Voce \*\*\*** | **0** | **24** | **0** | **Grade\*\*\*** | **24** |
|  |  | **Total** | |  |  | **24** |

**\*For each of the following three courses student can opt any one subject from Program Elective I or Program Elective II.**

|  |  |  |
| --- | --- | --- |
| **Course** | **Program Elective – I** | **Program Elective – II** |
| **MMVD 301** | **Micro Electro Mechanical Systems (MEMS)** | **RF Microelectronics** |
| **MMVD 302** | **Embedded System Design using ARM** | **Digital System Testing and Fault Simulation** |
| **MMVD 303** | **Nano Science & Technology** | **Digital Signal Processing in VLSI** |

\*\* Note: Minor project will be a kind of open ended problem based project. Topic/Title will be chosen by the students in the relevance of the studied courses during M.Tech.(MMVD). The evaluation for Minor Project will be based on the presentation /Viva-Voce given by student to examiners appointed by the PG Board of studies.

In theory papers, the internal assessment will be based on two class tests, one assignment and attendance in the class as per the classification given in academic ordinance for M.Tech. Courses. Where two teachers are teaching the subject, average of the tests and assignments will be considered.

\*\*\* The Project report & Viva- Voce examination of IV semester will be awarded grades only as per the following University norms. These grades will not be included in overall merit of M.Tech. (Microelectronics & VLSI Design) degree or CGPA and will be considered in SGPA only. These grades would be reflected in M.Tech. DMC along with Project Title.

|  |  |  |
| --- | --- | --- |
| Letter Grade | Grade Point | Marks |
| O (Outstanding) | 10 | 85-100 |
| A+ (Excellent) | 9 | 75-84 |
| A ( Very Good) | 8 | 65-74 |
| B+ ( Good) | 7 | 55-64 |
| B (Above Average) | 6 | 50-54 |
| C ( Average) | 5 | 41-49 |
| P (Pass) | 4 | 40 |
| F ( Fail) | 0 | Less than 40 |
| Ab | 0 | Absent |

MMVD 101 - Process Technology for ULSI – I

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100

Credits=4

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course Objective: Students should be able

1. To be able to learn the concepts of clean room environment for Fabrication of integrated circuits.
2. Students should have knowledge of cleaning process for silicon and other wafers for IC fabrication
3. Students should be able to learn process integration flow for different IC fabrication technologies.

Course Outcome:Students would be able

1. To describe various clean room technology for IC fabrication processes.
2. To describe steps in cleaning of silicon and other wafers.
3. To explain different IC fabrication technologies.

Course content

Unit I

Clean Room Technology, Clean Room Classifications, Design concepts, Clean Room Installations and Operations, Automation related facility systems, future trends.

Unit II

Wafer Cleaning Technology - Basic Concepts, Wet cleaning, Dry cleaning, Epitaxy, Fundamental Aspects, Conventional silicon epitaxy, low temperature, Epitaxy of silicon, selective epitaxial growth of Si, Characterization of epitaxial films.

Unit III

Process simulation, Introduction, Ion-implantation, Monte Carlo method, Diffusion and Oxidation, two-dimensional LOCOS simulation example, Epitaxy, Epitaxial doping model, Lithography, Optical projection lithography, Electron-beam lithography, Etching and deposition, future trends.

Unit IV

VLSI Process Integration, Fundamental considerations for IC Processing, building individual layer, integrating the process steps, miniaturizing VLSI circuits, NMOS IC technology, fabrication process sequence, special consideration for NMOS ICs, CMOS IC technology, Fabrication Process sequence, special considerations for CMOS ICs, MOS memory IC technology, dynamic memory, static memory, bipolar IC technology, fabrication process sequence, special considerations for bipolar ICs, Self-aligned bipolar structures, Integrated injection logic, IC fabrication, process monitoring future trends.

References:

1. VLSI Technology by S.M.Sze.
2. ULSI Technology by C.Y. Chang and S.M. Sze (McGraw Hill International)

MMVD 102 – MOSFET Physics and Sub-Micron Device Modeling

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100,

Credits=4,

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course Objective: Students should be able to

1. To understand semiconductor electronic properties based on energy band structure.
2. To learn basics of electron and hole concentrations and Fermi level in semiconductors.
3. To have knowledge of energy band diagrams for semiconductor structures and devices.
4. To understand I-V and C-V characteristics of MOS.
5. To learn second order effects of MOSFET.
6. To understand second order effects of MOSFET using CAD tools.

Course Outcomes: Students would be able to

1. Analyze semiconductor electronic properties based on energy band structure
2. Compute electron and hole concentrations and Fermi level in semiconductors.
3. Construct energy band diagrams for semiconductor structures and devices
4. Analyze and design I-V and C-V characteristics of MOS.
5. Simulate second order effects of MOSFET using CAD tools.

Course content

Unit I

Metal Semiconductor contacts – idealized Metal, Semiconductor junction, current voltage characteristics of schottky barrier, ohmic contacts, surface effects, MOS electronics, capacitance of the MOS system, non-ideal MOS system. Basic MOSFET behavior, Channel length modulation, Body bias effect, Threshold voltage adjustment,Sub threshold conduction.

Unit II

Limitation of long channel analysis, short channel effects, mobility degradation, velocity saturation, drain current in short channel MOSFETS, MOSFET scaling and short channel model, CMOS devices,MOSFET scaling goals , gate coupling, velocity overshoot, high field effects in scaled MOSFETs, substrate current, hot carrier effects, effects of substrate current on drain current, gate current in scaled MOSFETS.

Unit III

Moore law, Technology nodes and ITRS, Physical & Technological Challenges to scaling, Nonconventional MOSFET – (FDSOI, SOI, Multi-gate MOSFETs).

Unit IV

Numerical Simulation, basic concepts of simulations, grids, device simulation and challenges.

Importance of Semiconductor Device Simulators - Key Elements of Physical Device Simulation, Historical Development of the Physical Device Modeling.Introduction to the Silvaco ATLAS Simulation Tool, Examples of Silvaco ATLAS Simulations – MOSFETs and SOI.

References:

1. Device Electronics for Integrated circuits by muller and kammins.

2. Computational Electronics by DragicaVasileska and Stephen M. Goodnick.

3. Silicon Nanoelectronics – Shundri Oda & David Ferry, CRC Press

MMVD 103 - VLSI Design

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100

Credits=4

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course Objective: Students should be able

1. To Understand design methodologies and techniques applicable to VLSI technology.

2. To learn logic circuit layouts for both static CMOS and dynamic clocked CMOS circuits

3. To able to understand in sight of current developments in VLSI technology.

Course Outcome: Students would be able

1. To design Layout, Stick diagrams and learns Fabrication steps, Static and Switching characteristics of inverters.

2. To calculate the capacitance of a MOS capacitor.

3. To design digital systems using MOS circuits.

4. To aware about the trends in semiconductor technology, and how it impacts scaling and performance.

5. To describe leakage sources and reduction techniques in circuits using MOS.

Course Content

Unit I

Transistors and layouts - Transistors, Wires and Vias, Design Rules, Layout Design and Stick Diagrams - example, Logic Gate – Pseudo NMOS, DCVS, Domino. Delay through Resistive Interconnect. CMOS Inverter: Basic Circuit and DC Operation – DC Characteristics.

Unit II

Inverter Switching Characteristics- Static behavior– Switching threshold, Noise Margin, CMOS Inverter Dynamic Behavior- capacitances, propagation delay - High-to-Low time, Low to High time, Sources of Power Consumption, Power Consumption Static and dynamic. Logic Gate - Switch Logic.

Unit III

Combinational Logic Design- Standard cell based layout, CMOS Logic Circuits – CMOS NOR, NAND, Combinational network delays – Fan out, path delay, transistor sizing, cross talk minimization, power optimization. CMOS Transmission Gate (Pass gates). Sequential Logic design – Setup and hold time, SR latch circuit, clocked latch and flip flop circuits.

Unit IV

Sub system design, Design Principles, Adders, ALUs, High Density Memory, ROM, Static RAM case study of 4-M bit SRAM. FPGAs, PLAs. Floor Planning, Methods of Floor Planning, Chip Connections.

References:

1. Modern VLSI Design Systems on Silicon by Wayne Wolf (Pearson Education Asia)
2. CMOS Digital Integrated circuits- Analysis and design by Sung- Mo Kang and Yusuf Leblenici - MGH
3. Digital Integreted Circuits-(A design perspective) Jan M. Rabaey-P.M.I
4. Basic VLSI design-(Systems and Units (2nd edition) Pucknell & Eshraghian (PHI)
5. CMOS/BiCMOS VLSI by Yeo (Pearson).

MMVD 104 - Digital Signal Processing

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100

Credits=4,

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course Objective: Students should be able

1. To understand the basic concepts and techniques for processing of signals and systems.
2. To familiar with the most important methods in DSP.
3. To have knowledge of transform-domain processes on signals.
4. To learn basics of digital filter design.

Course Outcome: Students would be able

1. To represent discrete-time signals analytically and visualize them in the time domain.
2. To describe the meaning and implications of the properties of systems and signals.
3. To compute the Transform domain analysis of signals.
4. To understand the basics of digital filter design.

Course Content

Unit-I

Characterization and Classification of signals, typical signal processing operation. Examples of typical signals, Typical signal Processing Applications, Need of Digital Signal Processing.

Unit-II

Time Domain Representation of Signals and System- Discrete time signals, Operation on sequences, Discrete time systems, Time domain characterization of LTI Discrete- time systems, State-space Representation of LTI Discrete Time Systems.

Unit-III

The Discrete-Time Fourier Transform, Discrete Fourier Transform, Discrete Fourier Transform Properties, The z-transform, The inverse z-transform, Properties of z transform, Transform Domain Representations of LTI Systems- The frequency Response, transfer function.

Unit-IV

Digital Filter Structure- Block diagram Representation, signal-flow-graph representation, equivalent structures, Basic FIR Digital Filter Structures, Basic IIR Filter structures. Digital Filter Design- Low Pass IIR Digital Filter Design Examples

References:

1. Digital Signal Processing by Sanjit K.Mitra (TMH)

2. Digital Signal Processing by [S. Salivahanan](http://www.google.co.in/search?tbo=p&tbm=bks&q=inauthor:%22S.+Salivahanan%22), [A. Vallavaraj](http://www.google.co.in/search?tbo=p&tbm=bks&q=inauthor:%22A.+Vallavaraj%22), Tata McGraw-Hill.

3. Digital Signal Processing by John G. Prokais and [Dimitris K Manolakis](http://www.amazon.com/s/ref=ntt_athr_dp_sr_2?_encoding=UTF8&field-author=Dimitris%20K%20Manolakis&ie=UTF8&search-alias=books&sort=relevancerank) (Pearson)

4. Introduction to Digital Signal Processing by Johnson (PHI)

5. Digital Signal Processing: Theory, Analysis and Digital Filter Design by Nair (PHI)

MMVD 105 - Lab Work I

Maximum Marks: 100 Mark

Internal Assessment: 40 Marks,

External Practical Viva-Voce: 60 Marks

Credits: 8

Course Objective: Student should be able

1. To learn cleaning of silicon wafers and physical vapor deposition of various metals on substrates.
2. To understand the processes involved in fabrication of MOSFET.
3. To have knowledge of design and TCAD simulation of MOSFET at circuit level.
4. To learn basics of LINUX and C programming.
5. To have knowledge of MATLAB coding and simulation of various digital signal processes.
6. To understand basic analog circuit simulation using LT-SPICE.

Course Outcome:Student would be able

1. To do hands-on training on cleaning of silicon wafers and physical vapor deposition of various metals on substrates.
2. To simulate the processes involved in fabrication of MOSFET.
3. To design and TCAD simulation of MOSFET at circuit level.
4. To do coding of C language using basics LINUX command.
5. To do MATLAB coding and simulation of various digital signal processes.
6. To do basic analog circuit simulation using LT-SPICE

Course Content

Perform all the following experiments:

1. Cleaning and testing of silicon wafer and Metallization for contacts.
2. Design & Process Simulation of MOSFET using Athena.
3. Design and simulation of MOSFET inverters using VTCAD.
4. Familiarization with basic Linux commands and C Programming.
5. Coding of basic digital signal processes using OCTAVE/MATLAB.
6. Circuit simulation using LT-SPICE

MMVD 201 - Process Technology for ULSI-II

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100

Credits=4,

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course Objective: Students should be able

1. To acquire essential knowledge of rapid thermal processes and its advantages and disadvantages.
2. To understand different deposition technologies for thin layer depositions.
3. To have knowledge of different lithographic techniques.
4. To learn different material etching and metallization techniques.

Course Outcome: Students would be able

1. To describe rapid thermal processes, their advantages and disadvantages.
2. To explain fundamentals of different deposition techniques for thin film deposition.
3. To explain the basics of lithography and application of different lithographic technologies in IC fabrication processes.
4. To elaborate etching and metallization process and its significance in IC fabrication process.

Course Content

Unit I

Conventional Rapid thermal processes, Requirement for thermal processes, Rapid thermal processes, Future trends. Dielectric and Poly silicon film deposition processes, Atmospheric pressure CVD and low pressure CVD based silicon oxide, LPCVD Silicon Nitrides, LPCVD Poly Si Films, Plasma assisted depositions.

Unit II

Other deposition methods, Applications of deposited poly Silicon, Silicon oxide and Silicon nitride films. Lithography, Optical, Electron, X-Ray, Ion lithography

Unit III

Etching, Low pressure gas discharge, etch mechanism, selectivity and profile control, Reactive plasma etching techniques and equipment, Plasma based processes, diagnostics and point control and damage, wet chemical etching. Metallization, Metal deposition techniques, Silicide Process.

Unit IV

CVD Tungsten Plug, Other plug processes, Multi-level metallization, Metallization Reliability. Process Integration, Bi CMOS technology, MOS Memory technology, Process Integration Considerations. Assembly and packaging: introduction.

References:

1. ULSI Technology by C.Y. Chang and S. M. Sze (McGraw Hill International)

MMVD 202 - Embedded System Design using 8051

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100

Credits=4

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course Objective: Students should

1. Have knowledge about the basic structure and functions of embedded systems.
2. Have knowledge about the basic concepts and architecture of 8051 microprocessor.
3. Have knowledge of assembly language programming used for embedded system design.
4. Have knowledge of 8051 interfacing with external world.
5. Have knowledge of RTOS basics, uses, and relevance in embedded system design.

Course Outcome: Students would be able

1. To understand the basic of Embedded System Design.
2. To visualize the role of CISC & amp; RISC in processor operation.
3. To differentiate between embedded processor and other general purpose processors and how to use them in specific application.
4. To describe the architecture of 8051 micro-controller.
5. To use assembly language in registers, internal/external data moves, push and pop opcodes, data exchange, Logical Operations, Arithmetic Operations, Jump and Call Instructions.
6. To understand the Real world interfacing with 8051 with examples.
7. To understand RTOS – basics and relevance in embedded system.
8. To list Issues involved in embedded system design.

Course Content

Unit I

Embedded systems – introduction, role of processor and other hardware units, real-life examples, embedded systems on chip, Introduction to CISC and RISC architecture. Structural units of processor, processes selection for embedded system, memory devices for embedded systems and allocation of memory, DMA, interfacing memory, processor and I/O devices.

Unit II

Devices for embedded systems: I/O devices, timer and counting devices, Microprocessor and Micro controllers: differences, 8-bit micro controllers - comparison. Types of microcontrollers.The 8051 architecture: microcontroller hardware, I/O pins, ports and circuit, external memory, counter & timer, serial data input/output, interrupts.

Unit III

Programming of 8051 – instruction syntax, addressing modes, external data moves, code memory read-only data moves, push and pop opcodes, data exchange, logical operations, arithmetic operation, jump and call instructions. Case studies: pulse generator/ PWM, Digital Lock, Stepper motor control.

Unit IV

Real word interfacing with 8051: external memory, 8255, ADC, DAC. RTOS – basics and relevance in embedded system, typical applications hardware – software co-design in an embedded system: project management, design and co-design issues in system development process, design cycle, emulator and in-circuit emulator (ICE), use of software tools for development of an embedded system, issuers in embedded system design.

References:

1. Raj Kamal, Embedded Systems, Architecture, Programming and Design, TMH, 2003

2. The 8051 microcontroller – by Ayala (Penram)

3. Programming and Customizing the 8051 Microcontroller by Predko, Myke,, TMH, 2003

4. The 8051 MicroController& Embedded systems by MA. Mazidi & JG. Mazidi(Pearson)

5. Designing Embedded H/W By John Catsoulis (O’Reilly)

MMVD 203 - Analog CMOS Integrated Circuits

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100

Credits=4,

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course Objective: Students should be able

1. To understand the operation of CMOS devices, familiar with the small- and large-signal models of CMOS transistors,

2. To learn basics of current mirrors, operational amplifiers and voltage references.

3. Understand the concept of different parameters like gain, power, and bandwidth.

4. To understand the Switched capacitor circuits and data converters.

Course Outcome: Students would be able

1. To demonstrate the use of analog circuit analysis techniques to analyze the operation and behavior of various analog integrated circuits.

2. To demonstrate their knowledge by designing analog circuits.

3. To compute the gain, power, and bandwidth of analog circuits.

Course Content

Unit I

Introduction to analog design, Why analog, why CMOS ,Levels of abstraction, Robust analog design, MOS models, long channel v/s short channel, Analog layout, short channel considerations, Matching, Resistor layout, Noise considerations, Latchup.

Unit-II

Single stage amplifier, Basic concepts, Common source stage, Source follower, common gate stage, Band gap reference, Folded cascode, Differential amplifiers, Single ended and differential operation, common mode response Differential pair with MOS loads, Gilbert Cell.

Unit III

Current mirror, Cascode Current mirrors, Active Current mirror, Operational Amplifiers, One stage and two stage Op Amps, Gain boosting, Comparison, Common-mode Feedback, Input Range limitations, stability and frequency compensations, Comparator using OPAMPs (brief).

Unit IV

Switched capacitor circuits, Basic operation and analysis, switched Capacitor Gain Circuits; Data Converter fundamentals, Ideal D/A converter, Quantization noise, signed codes, performance limitations.

References:

1. Analog integrated circuit Design, David A. Johns & Ken Martin - John- Wiley &Sons, Inc. New York.

2. Design of Analog CMOS integrated circuits Behzad Razavi McGraw-Hill International edition.

3. CMOS: Circuit Design, layout, and simulation, R. Jacob, Baker and David E. Boyce, Prentice Hall of India.

4. Applications and Design with analog integrated circuits, 2 nd Edition - J. Michael Jacob, Prentice Hall of India.

5. Design and applications of analog Integrated Circuits, Prentice Hall of India,

MMVD 204 Verilog - Hardware Description Language

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100

Credits=4,

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course Objective: Students should be able

1. To differentiate between combinational and sequential circuits.

2. To design state machines to control complex systems.

3. To define and describe digital design flows for system design and recognize the trade-offs involved in different approaches.

4. To write synthesizable Verilog code.

5. To write Verilog test bench to test Verilog modules.

6. To Target a Verilog design to an FPGA board.

Course Outcome: Students would be able to

1. Describe various abstraction levels of Verilog HDL in modeling digital hardware.  
2. Explain modeling, simulation, and synthesis using the Verilog hardware description language.

3. Develop program codes for structural and behavioral modeling of combinational and sequential logic using Verilog HDL.

4. Describe the role of hardware description language (HDL) in design flows for FPGA and ASIC.

5. Describe the role of Verification in digital hardware development.

6. Develop various test cases for simulation.

Course Content

Unit I

Verilog: Overview of Digital Design with Verilog HDL, Concepts of CPLD and FPGA, Hierarchical Modeling, Basics of Verilog - Data Types, System Tasks and Compiler Directives, Modules and Ports, Gate Level Modeling- Gate Types, Gate Delays.

Unit II

Behavioral Modeling - Structured Procedures, Procedural Assignments, Timing Controls, Conditional Statements, Multiway Branching, Loops, Sequential and Parallel Blocks, Tasks and Functions – Exercises. FSM based HDL design-Moore & Mealy machines.

Unit III

Useful modeling techniques- Procedural continuous assignments, overriding parameters, conditional compilation and execution, time scales, useful system tasks, Advance Verilog Topics- Timing and delays – types of delay models, path delay modeling, Timing checks, delay back-annotation, Switch level modeling – switch modeling elements, examples.

Unit IV

Logic Synthesis with Verilog HDL- What is logic synthesis, impact of logic synthesis, Verilog hdl synthesis, synthesis design flow, RTL to gates (Example, Verification of gate level net list, modeling tips for logic synthesis, examples of sequential circuit synthesis.

References:

1. Verilog HDL - Samir Palnitkar (Pearson)
2. Verilog HDL Synthesis, A Practical Primer – J Bhasker
3. Digital Design: With an Introduction to Verilog HDL - [M. Morris Mano](http://www.amazon.in/s?_encoding=UTF8&field-author=M.%20Morris%20Mano&search-alias=stripbooks)
4. Design Through Verilog HDL - B.Bala Tripura Sundari T.R. Padmanabhan
5. FSM based HDL Design –Peter Minns, lan Elliott(Wiley)

MMVD 205 - Lab Work II

Maximum Marks: 100 Mark

Internal Assessment: 40 Marks,

External Practical Viva-Voce: 60 Marks

Credits: 8

Course Objective: Students should be able

1. To learn the various processes involved in fabrication of MOS capacitor and its characteristics.
2. To understand the fabrication of MOS capacitor and its characterization.
3. To write code for different digital circuits using HDLs.
4. To learn advanced level analog circuits using LT-SPICE.
5. To have knowledge of assembly language programming of 8051.
6. To have basic knowledge of interfacing of 8051 with external circuits.

Course Outcome: Students would be able

1. To simulate the different processes involved in MOS capacitor fabrication and its characterization.
2. To perform hands-on practice on the MOS capacitor fabrication and its characterization.
3. To simulate and synthesize of different digital circuits using hardware description languages.
4. To acquire skills and knowledge of LT-SPICE simulation of advanced analog circuits.
5. To do basic programming of 8051 using assembly languages.
6. To interface 8051 with basic external devices.

List of experiment

1. Design and simulation of MOS capacitor using Athena Process Simulation tool.
2. Fabrication and Characterization of MOS capacitor (I-V, C-V).
3. Write, simulate and demonstrate Verilog model code for various Digital circuits.
4. Advanced Analog Circuit simulation using LT-SPICE.
5. Data flow and arithmetic logical operations programs in assembly language.
6. “Interfacing of 8051 with external world” programs using assembly or embedded C

MMVD 301 (Program Elective - I) Micro Electro Mechanical Systems (MEMS)

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100

Credits=4,

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course Objective: - Students should be able

1. To understand basic concepts of MEMS technology and requirement of materials for MEMS.

2. To learn different micromachining techniques for MEMS device fabrication.

3. To have knowledge of design and simulation of MEMS devices using CAD tools.

Course Outcome**:** Students would be able

1. To explain the fundamental concept of MEMS technology, its significance and the different materials used for this technology.

2. To implement the knowledge of MEMS device fabrication using different micromachining processes.

3. To use CAD tools for the simulation of MEMS devices.

Course Content

Unit I

Overview of MEMS and Microsystems: Introduction Microsystem vs. MEMS, Microsystems and Microelectronics, the Multidisciplinary Nature of Microsystem design and manufacture, Application of MEMS in various industries. MEMS and Miniaturization: Scaling laws in miniaturization: Introduction to Scaling, Scaling in: Geometry, Rigid Body dynamics, Electrostatic forces, Electromagnetic forces, Electricity, Fluid Mechanics, Heat Transfer. Materials for MEMS and Microsystems – Si as substrate material, mechanical properties of Silicon, Silicon Compounds (SiO2, Si3N4, SiC, polySi, Silicon), Piezoresistors, GaAs, Piezoelectric crystals, Polymers, Packaging Materials.

Unit II

Micromachining Processes: Overview of microelectronic fabrication processes used in MEMS, Bulk Micromachining – Isotropic & Anisotropic Etching, Comparison of Wet vs Dry etching, Surface Micromachining – General description, Processing in general, Mechanical Problems associated with Surface Micromachining, Introduction to LIGA process, and Introduction to Bonding. Assembly of 3D MEMS - foundary process.

Unit III

Microsystems & MEMS Design: Design Considerations: Design constraints, Selection of Materials, Selection of Manufacturing processes, Selection of Signal Transduction, Electromechanical system, packaging. Process design, Mechanical Design – Thermo mechanical loading, Thermo mechanical Stress Analysis, Dynamic Analysis, Interfacial fracture Analysis, Mechanical Design using Finite Element Method.

Unit IV

Design case using CAD. Principles of Measuring Mechanical Quantities: Transduction from Deformation of Semiconductor Strain gauges: Piezo resistive effect in Single Crystal Silicon, Piezo resistive effect in Poly silicon Thin films, Transduction from deformation of Resistance. Capacitive Transduction: Electro mechanics, Diaphragm pressure sensors. Structure and Operation of Accelerometers, Resonant Sensors, Thermal Sensing and actuation.

References:

1. Microsystem Design By Stephen D. Senturia, Kluwer Academic Publishers (2003)
2. Micro Technology and MEMS By M. Elwenspoek and R. Wiegerink, Springer (2000)
3. Micro Fabrication by Marc Madaon, CRC Press
4. MEMS & Microsystems Design and Manufacture by Tai-Ran H Su, Tata Mc graw.

MMVD 301 (Program Elective - II) RF Microelectronics

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100

Credits=4,

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course Objective: Students should be able

1. To understand RF technology, wireless technology and their application in IC design technology
2. To have knowledge of RF network analysis
3. To learn noise optimization in RF circuits.
4. To have knowledge of different RF microelectronics chips for various application.

Course Outcome: Students would be able

1. To explain RF technology, wireless technology and their application in IC design technology
2. To perform RF network analysis
3. To design noise optimization in RF circuits.
4. To design different RF microelectronics chips for various application.

Course Content

Unit I

Importance of RF and wireless technology, IC design technology for RF circuits RF Behavior of passive components, operation for passive components at RF Active RF Components, RF Diodes, RF BJTs, RF FET, HEMT Active RF component modelling, Transistor models.

Unit-II

Circuit representation of two port RF / Microwave Networks, Low and high frequency parameters, Formulation and properties of s parameters, Shifting reference plans, Transmission matrix, Generalized scattering parameters, Passive Circuit design, Review of Smith chart Matching and Biasing networks, Impedence matching using discrete components, microstrip line matching networks, amplifier classes of operation, RF Transistor amplifier designs, Low Noise amplifiers, Stability consideration, Constant gain noise figure circles.

Unit III

Noise considerations in active networks, Noise definition, noise sources. RF / Microwave oscillator design, Oscillator versus amplifier design, Oscillation conditions, Design of transistor oscillators, Generator Tuning networks RF / Microwave Frequency conversion II: Mixer design, Mixer types, Conversion loss for SSB mixers, SSB mixer versus DSB mixers. One diode mixers, two diode mixers,

Four diode mixers, eight diode mixers,

Unit IV

Frequency synthesizers, PLL, RF synthesizer architectures, Transceiver architectures, Receiver architectures, Transmitter architectures, RF / Microwave IC design, Microwave ICs, MIC Materials, Types of MICs, Hybrid vs monolithic MICs, Case studies, Relating to design of different circuits employed in RF Microelectronics.

References:

1. Behzad Razavi, “RF Microelectronics” Prentice Hall PTR , 1998
2. R.Ludwig, P.Bretchko, RF Circuit Design, Pearson Education Asia, 2000.
3. Matthew M. Radmanesh, Radio Frequency and Microwave Electronics Illustrated, Pearson Education (Asia) Ltd., 2001

MMVD 302 (Program Elective - I) Embedded System Design using ARM

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100

Credits=4,

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course Objective: Students should

1. Have knowledge about the basic structure and functions of embedded systems.
2. Have knowledge about the basic concepts and architecture of ARM processor.
3. Have knowledge of assembly language programming used for embedded system design.
4. Have knowledge of ARM cache management.
5. Have knowledge of RTOS basics, uses and relevance in embedded system design.

Course Outcome: Students should be able

1. To understand the basics of ARM processor.
2. To describe ARM architecture.
3. To explain instruction set, modes and interrupts in ARM.
4. To do simple programming in ARM.
5. To explain the cache mechanism in ARM Processor.
6. To understand the Memory management Unit of ARM.
7. To understand RTOS – basics and relevance in embedded system.

Course Content

Unit I

ARM processor architecture: the risc and ARM design philosophy, embedded system hardware. ARM processor fundamentals: data flow model, registers, modes of operation, current program status register, pipeline, exceptions, interrupts, and arm families.

Unit II

ARM instructions sets and interrupts: arm and thumb instruction sets, data processing instructions, branch instructions, load- store instructions, software interrupt instruction, program status register instructions, conditional execution, stack instructions, software interrupt instruction. ARM processor exceptions and modes: vector table, priorities, link register offsets, interrupts, and irq / fiq exceptions interrupt stack design and implementation. Simple program: addition, subtraction, and multiplication in assembly

Unit III

Cache mechanism: introduction to cache memory, memory hierarchy and cache memory, cache architecture and cache policies. Concept of flushing and cleaning cache: flushing and cleaning arm cache core. Concept of cache lockdown: locking code and data in cache. Cache and write buffer

Unit IV

Memory management unit: how virtual memory works, details of the arm mmu, page tables, translation look-aside buffer, domains and memory access permissions. Embedded os and rtos: fundamental components to embedded os, simple little operating system: initialization, memory model, interrupts and exceptions handling, scheduler. Introduction to rtos: real-time systems concepts, foreground/background systems, critical sections, resources, multitasking, context switching, scheduling, re-entrancy, task priorities.

References:

1. “ARM System Developer’s Guide Designing and Optimizing” by Andrew N.Sloss Elsevier publication, 2004.
2. “MicroC/OS – II” second edition The Real Time Kernel Jean J. Labrosse Publisher: Viva Books Private Ltd (Feb 2002)
3. “Embedded systems” B.Kanta Rao PHI publishers, Eastern Economy Edition, 2011
4. “Embedded Systems Architecture” - Tammy Noergard, Newness edition, 2005
5. “ARM System-on-Chip Architecture” 2nd Edition, Steve Furbe, Pearson Education, 2000
6. “Embedded/Real Time Systems” Dr. K.V.K.K Prasad Dream tech press, 2009.

MMVD 302 (Program Elective II) - Digital System Testing and Fault Simulation

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100

Credits=4,

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course Objective: Students should

1. Have knowledge of digital system testing.
2. Have knowledge of simulation methods for fault testing.
3. Have introduction to various fault models like Functional Faults, Structural Faults, and Structural Gate Level Faults.
4. Have basic knowledge of various designs for testability techniques.

Course Outcome: Students would be able

1. To describe basic concepts of digital system Testing.
2. To understand the functional fault modeling at logic level as well as register level.
3. To learn various simulations methods used for fault testing.
4. To describe various fault models like Functional Faults, Structural Faults and Structural Gate Level Faults.
5. To understand various Automatic Test Generation algorithms for Single stuck Faults.
6. To apply various design for test-ability techniques.

Course Content

Unit I

Functional Modeling at the logic Level, Functional Modeling at the Register Level, Structural Models, Level of Modeling, Types of Simulation, Compiled Simulation, Event-Driven Simulation, Delay Models. Basic of Test and role of HDLs in testing (Introduction only), Verilog HDL for Design and Test in combinational circuits and sequential circuits.

Unit II

Fault Modeling:- Fault Abstraction, Functional Faults, Structural Faults, Structural Gate Level Faults, Recognizing Faults, Stuck-Open Faults, Stuck-at-0 Faults, Stuck-at-1 Faults, Bridging Faults, State-Dependent Faults, Multiple Faults, Single Stuck-at-Structural Faults, Detecting Single Stuck-at Fault, Detecting Bridging Faults, Fault Collapsing, Dominance Fault Collapsing, Fault Simulation:-Gate-Level Fault Simulation.

Unit III

Testing for single step faults - Basic Issues, ATG algorithms for SSFs in Combinational Circuits: D, 9-V, PODEM Algorithms, Fault independent test generation, Sequential Circuit test generation,

Unit IV

Design for Test, Testing Sequential and Combinational Circuits, Ad Hoc Design for Testability Techniques, Testability insertion - Controllability and Observability concept, Full Scan Insertion, Flip - Flop Structures, General Aspects of Compression Techniques, Ones-Count Compression, LFSR used as signature analyzer , Introduction to BIST and MBIST.

References:

1. Digital systems testing and testable design – Miron Abramovici, Computer Science Press (1991).
2. Digital System Test and Testable Design: Using HDL Models and Architectures by [Zainalabedin Navabi](http://www.amazon.in/s?_encoding=UTF8&field-author=Zainalabedin%20Navabi&search-alias=stripbooks).
3. Test generation for VLSI chips by VD Agrawal and SC Seth, IEEE Computer Society Press (2003).
4. Essentials of Electronic Testing by ML Bushnell, VD Agrawal, Kluwer Academic Publishers.
5. VLSI Testing: digital and mixed analogue digital techniques Stanley L. Hurst Pub (1999).

MMVD 303 (Program Elective -I) Nano Science and Technology

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100

Credits=4,

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course objective: students should be able

1. To understand the fundamental forces controlling the dynamic and static response of materials at the Nano- scale.  
2. To have comprehensive understanding of state-of-the-art Nano-fabrication methods.  
3. To have knowledge of processing conditions to functional nanomaterials.  
4. To scalable system for the continuous production of nanomaterials.  
5. To understand the state-of-the-art characterization methods for nanomaterials.

Course outcome: students would be able

1To explain the fundamental forces controlling the dynamic and static response of materials at the Nano-scale.  
2. To demonstrate a comprehensive understanding of state-of-the-art Nano-fabrication methods.  
3. To determine and evaluate processing conditions to functional nanomaterials.  
4. Design and analyse scalable system for the continuous production of nanomaterials.  
5. To Practice and explain the state-of-the-art characterization methods for nanomaterials.

Course Content:

Unit I

Introduction to Nanotechnology and Nano materials, History, ethical issues, applications in different fields, bottom up and top down approaches, Introduction to Zero, One and Two Dimensional Nanostructures, Quantum devices: Resonant tunneling diode, Coulomb Blockade, Single Electron Transistor.

Unit II

Nano Material Synthesis techniques Physical methods: ball milling, Atomic Layer Deposition, Molecular beam epitaxy , spray pyrolysis, Chemical Methods: Sol gel, self-assembly, Chemical Vapor depositions, template manufacturing, biological synthesis.

Unit III

Carbon nanotubes, structures and synthesis, growth mechanism and properties, devices applications, Nanowires: synthesis and characterization, Molecular Switches and logic gates. Nano manipulation and nano lithography: E-beam and nano imprint lithography.

Unit IV

High resolution nano lithography, Dip-Pen lithography, AFM Lithography. Nano characterization: High Resolution TEM, Scanning Probe Microscopes: Atomic Force Microscope and Scanning Tunneling Microscope, Nano manipulator, Lab on a Chip concept.

References:

1. Nanotechnology: Principle and Practices by Sulbha Kulkarni

2. Hand book of Nanotechnology By Bhushan , Springer

3. Nano: The Essentials By T. Pradeep

3. Microfabrication by Marc Madaon, CRC Press

MMVD 303 (Program Elective -II) - Digital Signal Processing in VLSI

Instructions: There shall be eight questions in total, two from each unit. Students are required to attempt five questions, selecting at least one from each unit. All questions will carry equal marks.

Maximum Marks: 100

Credits=4,

Time = 3 hours

Internal Assessment: 40 Marks, Theory Exam: 60 Marks.

Course Objective: Student should be able

1. To understand Characterization and classification of signals, applications and need of DSP in VLSI.

2. To understand the concept of digital filters and FIR filters, their various types and comparison.

3. To have knowledge of time domain representation of discrete time signals and systems.

4. To understand various DSP algorithms used for VLSI applications.

5. To have knowledge of DSP in the field of VLSI like digital Transceiver; Digital detection, Digital heterodyning, decimation and interpolation. Real-time detection.

Course Outcome: Students would able

1. To explain the Characterization and classification of signals, applications and need of DSP in VLSI.

2. To visualize the concept of digital filters and FIR filters; their various types and comparison.

3. To apply time domain representation of discrete time signals and systems.

4. To elaborate various DSP algorithms used for VLSI applications. They should also be able to explain the DSP hardware and system related concepts.

5. To relate the knowledge of DSP in the field of VLSI like digital Transceiver; Digital detection, Digital heterodyning, decimation and interpolation. Real-time detection

Course Content

Unit I

Introduction, Review of signals and signals processing, Enhancement of S/N, system models and the transfer function, spectra, limitations of Analog systems. Digital Signal Processing: Flexibility, key advantage to DSP, DSP issues and terminology, Sampled Data, Throughput expansion, data compression and pipelining. Non-recursive filters: Finite impulse response filters; Digital filters Recursive filters: Analog feedback filters and their recursive digital counterparts, Digital filter in block diagram form.

Unit II

Digital Filter Overview: Digital filters, when, why, what, how? Comparison of digital filter types; summary of key digital filter relationships. FIR filters: FIR filter concepts and properties, Fourier-series approach to FIR filters; the window method of FIR filter design. FIR Filters: The second-order section as a prototype; Biquads for special purposes; Hardware implementation of FIR filters. The bridge to VLSI: Introduction, Some VLSI-DSP design Philosophy DSP, Architecture Issues: Tradeoffs, Pipelining, and parallelism.

Unit III

Finite-word length arithmetic-Introduction, Arithmetic error sensitivity, Overflow, underflow, and rounding; filter quantization-error tradeoffs in fixed-point arithmetic, Accuracy in FFT spectral Analysis. Analog I/O methods Real DSP Hardware: Introduction, key, DSP hardware elements, System Selection: DSP system alternatives; Microcoded systems; Single-chip DSP microprocessor survey.

Unit IV

DSP applications: Introduction, Major elements of a DSP system, the digital Transceiver; Digital detection, Digital heterodyning, decimation and interpolation. Real-time detection: Examples based on correlation principles, coherent detection modeling in Real time: Telecommunications and speech. Why modeling; Telecommunications; coding of speech. Image Processing: Introduction to image processing; Machine vision acquisition, enhancement, and recognition.

References:

1. Digital Signal Processing in VLSI by Richard J. Higgins (Prentice Hall)

MMVD 304 – Minor Project

Maximum Marks: 100

Credits=8

Time = 3 hours

Internal Marks: 0, External marks: 100

Minor Project Objective: Students should able

1. To carry out open ended minor project related to Microelectronics and VLSI design.
2. To present project findings and submit a technical report.

Minor Project Outcome: Students would able

1. To design, analyze, evaluate and simulate/ experimental work.
2. To do implementation of principles, procedures, laws, techniques, methods studied

MMVD 401 - Project Dissertation

Credits=24

Duration: 6 Months

Project Dissertation Objective: (Thesis): Students should able

1. To carry out work on an open ended research problem using appropriate techniques, tools and skills.
2. To come with new innovative idea, research problem.

Project Dissertation Outcome: (Thesis) Students would able

1. To design, analyze, evaluate and simulate/ experimental work.
2. To Present project findings and submit technical papers and dissertation.
3. To do implementation of principles, procedures, laws, techniques, methods studied.