Proposed Draft Syllabi

**Course: Bachelor of Science (B.Sc.)**

**Subject: Electronics**

**Examination Scheme**

1. Theory Papers(Semester System of Examination)
	1. Syllabus in each Theory Paper is divided in 4 units.
		1. A Student is required to attempt 5 questions in all.
		2. Question No 1 is compulsory, consisting of short answer type questions based on all the 4 units.
		3. Two questions will be set from each unit. A student is required to attempt one question from each unit.
		4. All questions carry equal marks.

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* + - 1. Use of simple calculator is permissible.
			2. Instructions should be imparted using SI system of units. Familiarity with CGS system of units should also be ensured.
			3. Distribution of Marks :

 Paper I –40+10\*= 50 marks of 3 hours duration.

 Paper II – 40+10\*=50 marks of 3 hour duration.

\* For each paper question paper will be of 40 marks and 10 marks in each theory paper are awarded through internal assessment in each semester.

5. Work load – 3 periods per week per theory paper

1. Practical Paper (Annual Examination System)
	1. The Practical examination will be held at the end of even semester in two sittings of three hours each with First sitting starting in the evening session of the first day and second sitting in the following morning session.
	2. A candidate is required to perform minimum of 6 experiments in each section out of the list provided during course of study in odd and even semester in corresponding session and is required to perform one experiment from each section in examination. Experiment from one section in First Sitting and experiment from other section in Second Sitting.
	3. Distribution of Marks :
		* 1. Paper III – 100 Marks of 3+3 Hours duration
			2. Lab Record: 20
			3. Experiments: 20 + 20
			4. Viva/Voce : 20+20
2. Maximum 10 students in one group during course of study and also in Examination.

v) Work Load – 6 periods per week per group.

Proposed Draft Syllabi w.e.f session 2018-19

**Course: Bachelor of Science (B.Sc.)**

**Subject: Electronics**

**Examination Scheme**

**B.Sc Electronics Course Study Cum Examination Scheme for Sem I &II**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Sem | Paper Code | Nomenclature Of Paper | InternalAssessment \* | Max.Marks | TotalMarks | PassMarks | Exam Duration | Work load | ExamSystem |
| I | Paper-1 | Electronic Devices and Circuits-I | 10 | 40 | 50 | 18 | 3 Hrs | 3 periods /week | Sem |
| Paper-2 | Network Analysis | 10 | 40 | 50 | 18 | 3 Hrs | 3 periods /week |
| II | Paper-1 | Electronic Devices and Circuits-II | 10 | 40 | 50 | 18 | 3 Hrs | 3 periods /week | Sem |
| Paper-2 | Digital Electronics-I | 10 | 40 | 50 | 18 | 3 Hrs | 3 periods /week |
| Common forSem I & Sem II | Paper-3 | ELECTRONICS | - | 100 | 100 | 35 | 3+3 Hrs | 6 periods /week | Annual |

1. Practicals classes to be conducted during odd as well as even semester.
2. The Practical examination will be held at the end of even semester in two sittings of three hours each with First sitting starting in the evening session of the first day and second sitting in the following morning session.
3. A candidate is required to perform minimum of 6 experiments in each section out of the list provided during course of study in odd and even semester in corresponding session and is required to perform one experiment from each section in examination. Experiment from one section in First Sitting and experiment from other section in Second Sitting.
4. Distribution of Marks :
	* + 1. Paper III – 100 Marks of 3+3 Hours duration
			2. Lab Record: 20
			3. Experiments: 20 + 20
			4. Viva/Voce : 20+20

5. Maximum 10 students in one group during course of study and also in Examination.

**Semester-I**

**Course: B.Sc**

**Subject: Electronics**

**Paper: I (Theory)**

**Nomenclature:-Electronic Devices and Circuits-I**

 **Unit –I**

**Introduction to Semiconductors:-** Intrinsic and Extrinsic semiconductors, Energy Band diagram, drift and diffusion currents in semiconductors (Basic idea only), Junction diode and its characteristics, Space charge capacitance and diffusion capacitance (Basic idea only), Zener diode, Voltage Regulation using Zener Diode (Basic Idea), Schottky diode , shunt and series clipping circuit., clamping circuit .

**Unit-II**

**Rectifiers:** - HWR, FWR, Bridge FWR, calculation of rectifier parameters.

Filter circuits: L, C, LC (Calculation of ripple factor), Voltage multiplier Circuit.

# Unit –III

**Bipolar Junction Transistor:-** Potential curves in unbiased and biased transistor, Transistor current components, Early effect, Static Characteristics of CB & CE configuration, active, cut off and saturation regions.

Transistor as an Amplifier, Transistor current gains (Alpha, Beta, and Gama)

**Unit-IV**

**Transistor Model: -** Ebers-moll model of transistor, Hybrid-Model of transistor, Emitter follower, calculation of transistor amplifier parameters using h-model, comparison of transistor amplifier configuration, millers – theorem and its dual

**Reference Books:**

1. Integrated Electronics by Millman and Halkias.
2. Basic Electronics and Linear Circuits by NN Bhargava, DC Kulshreshtha (TTTI)
3. Electronics Devices and Circuit By Allen Mottershead

**Note:**

* 1. Syllabus in each Theory Paper is divided in 4 units.
		1. A Student is required to attempt 5 questions in all.
		2. Question No 1 is compulsory, consisting of short answer type questions based on all the 4 units.
		3. Two questions will be set from each unit. A student is required to attempt one question from each unit.
		4. All questions carry equal marks.

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* + - 1. Use of simple calculator is permissible.
			2. Instructions should be imparted using SI system of units. Familiarity with CGS system of units should also be ensured.
			3. Distribution of Marks: 40+10\*.

\* Each theory question paper will be of 40 marks of 3 hours duration and 10 marks in each theory paper are to be awarded through internal assessment in each semester.

5. Work load – 3 periods per week per theory paper

Semester –I

**Course: B.Sc**

Subject: Electronics

**Paper: II (THEORY)**

**Nomenclature: -Network Analysis**

 **Unit-I**

**Network Theorems-I:-** Kirchoffs Voltage Law, Kirchoffs Current Law, Mesh Analysis, Nodal Analysis, Source Transformation Technique, Star-Delta Transformation, Superposition Theorem, Thevenin’s Theorem, Examples and problems of each topic.

**Unit-II**

**Network Theorems-II:-** Norton’s Theorem, Reciprocity Theorem, Compensation Theorem, Maximum Power Transfer Theorem, Duals and Duality, Tellegen’s Theorem, Millman’s Theorem.

**Unit –III**

**Two–port Network-I:-** Open Circuit Impedance(Z) Parameters, Short Circuit Admittance (Y) Parameters, Transmission(ABCD) Parameters, Inverse Transmission (A’B’C’D’) Parameters, Hybrid(h) Parameters, Inverse Hybrid(g) Parameters , Inter Relationships of different parameters.

**Unit –IV**

**Two–port Network-II: -** Conversion of Parameters, Inter Connection of Two – Port Networks, T and π Representation, Terminated Two-Port Networks, Lattice Networks, Image Parameters

**Reference Books:**

* + - 1. Circuits and Networks by A. Sudhakar, Shyammohan
			2. Network Analysis , Publication Khanna By G.K. Mithal
			3. Network Analysis , Publication Pearson India By M.E. Van Valkenburg

**Note:**

1. Syllabus in each Theory Paper is divided in 4 units.
2. A Student is required to attempt 5 questions in all.
3. Question No 1 is compulsory, consisting of short answer type questions based on all the 4 units.
4. Two questions will be set from each unit. A student is required to attempt one question from each unit.
5. All questions carry equal marks.

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2. Use of simple calculator is permissible.

3. Instructions should be imparted using SI system of units. Familiarity with CGS system of units should also be ensured.

4. Distribution of Marks: 40+10

\* Each theory question paper will be of 40 marks of 3 hours duration and 10 marks in each theory paper are to be awarded through internal assessment in each semester.

 5. Work load – 3 periods per week per theory paper

**Semester-II**

**Course: B.Sc**

**Subject: Electronics**

**Paper: I (Theory)**

**Nomenclature: - Electronic Devices and Circuits –II**

 **Unit-I**

**Transistor Biasing Techniques-I:-** Why Bias a Transistor, Selection of Operating Point, Need for Bias Stabilization, Requirement of a Biasing Circuit, Different Biasing Circuits: Fixed-Bias Circuit, Collector-to-base Bias Circuit.

**Unit-II**

**Transistor Biasing Techniques-II:-**  Bias Circuit with Emitter Resistor, Voltage Divider Biasing Circuit, Emitter-Bias Circuit, and Gain of a multi-stage amplifier.

**Unit-III**

**Coupling Techniques:-** How to couple two stages, Resistance-Capacitance Coupling, Transformer Coupling, Direct Coupling, Frequency Response Curve of an RC-Coupled Amplifier of two stage: Fall of Gain in Low-frequency Range, fall in gain of high Frequencies, Bandwidth of an amplifier.

**Unit-IV**

**Field Effect Transistor:-** Junctions Field Effect Transistor, Qualitative Description of JFET, Drain and transfer characteristics of JFET, FET small signal low frequency model, CS & CD low frequency model, MOSFET -Depletion and enhancement and their drain & transfer characteristics, CMOS( Basic idea).

**Reference Books:**

1. Basic Electronics and Linear Circuits by NN Bhargava, D C Kulshreshtha
2. Integrated Electronics by Millman and Halkian
3. Electronics Devices and Circuit By Allen Mottershead

**Note:**

1. Syllabus in each Theory Paper is divided in 4 units.

1. A Student is required to attempt 5 questions in all.
2. Question No 1 is compulsory, consisting of short answer type questions based on all the 4 units.
3. Two questions will be set from each unit. A student is required to attempt one question from each unit.
4. All questions carry equal marks.

.

2. Use of simple calculator is permissible.

3. Instructions should be imparted using SI system of units. Familiarity with CGS system of units should also be ensured.

4. Distribution of Marks: 40+10

 \* Each theory question paper will be of 40 marks of 3 hours duration and 10 marks in each theory paper are to be awarded through internal assessment in each semester.

 5. Work load – 3 periods per week per theory paper

**Semester-II**

**Course: B.Sc**

**Subject-Electronics**

**Paper: II (Theory)**

**Nomenclature:-Digital Electronics-I**

 **Unit-I**

**Number Systems:**- Binary, Octal, Hexadecimal number system and base conversions, Binary Arithmetic operations , 1’s and 2’s complement representation and their arithmetic, Binary codes-BCD, Grey, cyclic, ASCII, EBCDIC, Parity Bit Code, BCD arithmetic.

**Unit-II**

**Logic Gates and Boolean Algebra:-**Logic Level: Positive and Negative logic level, Logic Gates: AND, OR, NOT, XOR, XNOR, NOR, NAND (Definition, Symbols& Truth table).

Boolean Algebra: Postulates, Duality Principal , De Morgan’s Law, Simplification of Boolean Identities , Standard SOP & POS Forms, Simplification using K-map(upto 4 variables), don’t care condition, implementation of SOP & POS form using NAND and NOR Gate.

**Unit III**

**Logic families: -** Unipolar & Bipolar Logic families, characteristics of Digital IC’s (fan in, fan out, propagation delay. Noise Margin, level of Gating), RTL (NOR), DTL (NAND), TTL (NAND), CMOS Logic gate (NAND, NOR).

**Unit-IV**

**Combinational Circuit:-**Design principle of combinational circuit: Half adder, full adder, half subtractor, full subtractor, parallel binary adder, BCD (8421)adder, 2’S complement adder/ subtractor, Digital Comparator (1 bit and 2 bit ), Application of combinational circuit: railway track switching system , common light switching for a group of flats, Parity Generator.

**Reference Books:**

1. Digital Electronics by R.P. Jain
2. Digital Computer Electronics by Aalbert Paul Malvino.

**Note:**

1. Syllabus in each Theory Paper is divided in 4 units.

1. A Student is required to attempt 5 questions in all.
2. Question No 1 is compulsory, consisting of short answer type questions based on all the 4 units.
3. Two questions will be set from each unit. A student is required to attempt one question from each unit.
4. All questions carry equal marks.

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2. Use of simple calculator is permissible.

3. Instructions should be imparted using SI system of units. Familiarity with CGS system of units should also be ensured.

4. Distribution of Marks: 40+10.

\* Each theory question paper will be of 40 marks of 3 hours duration and 10 marks in each theory paper are to be awarded through internal assessment in each semester.

 5. Work load – 3 periods per week per theory paper

**SEMESTER 1 & 2**

**Course: B.Sc**

**SUBJECT: ELECTRONICS**

**PAPER: III (PRACTICAL)**

**Note:** A candidate is required to perform minimum of 6 experiments in each section out of the list provided during course of study in odd and even semester in corresponding session.

**Section-A**

1. Identification and study of Electronics Components.
2. To study the V-I characteristics of PN junction diode.
3. To study the zener diode as voltage regulator.
4. To study half wave voltage multiplier Ckt. Using diode.
5. To study HWR and FWR and measurement of ripple factor with and without C filter.
6. To study diode as shunt clipping clement.
7. To study diode as clamping element.
8. Study of CB characteristics and calculation of H parameter from graph.
9. Study of CE characteristics and calculation of H parameter from graph.
10. Study of JFET characteristics.
11. To measure Av. Ai. Ap. In CE Transistor amplifier.
12. Study of fixed bias arrangement for transistor.

**Section-B**

1. Measurement of voltage. Time period and phase-shift using CRO.
2. Study of basis logic gate (AOI).
3. Study of DTL NAND gate.
4. Study of TTL NAND gate.
5. Digital trainer using AOI.
6. Digital trainer using NAND.
7. To study RC Ckts. As integrating and differentiating Ckts.
8. To verify maximum power transfer theorem for DC network.
9. To study RC low pass filter and measurement of cut-off frequency from graph..
10. To study RC High pass Filter and measurement of cut-off frequency from graph..
11. To study the application of Superposition theorem.

 **Note:**

* 1. The Practical examination will be held at the end of even semester in two sittings of three hours each with First sitting starting in the evening session of the first day and second sitting in the following morning session.
	2. A candidate is required to perform minimum of 6 experiments in each section out of the list provided during course of study in odd and even semester in corresponding session and is required to perform one experiment from each section in examination. Experiment from one section in First Sitting and experiment from other section in Second Sitting.
	3. Distribution of Marks :
		+ 1. Paper III – 100 Marks of 3+3 Hours duration
			2. Lab Record: 20
			3. Experiments: 20 + 20
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1. Maximum 10 students in one group during course of study and also in Examination.

v) Work Load – 6 periods per week per group.