**Kurukshetra University, Kurukshetra**

**Syllabus and Scheme of Examination for Undergraduate Programme**

**Under**

**(Multiple Entry-Exit, Internship and CBCS-LOCF –NEP) w.e.f. 2022-23**

**Course: Electronics**

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| --- | --- | --- | --- | --- | --- | --- | --- |
| **Semester** | **Course** | **Paper No.** | **Nomenclature of paper** | **Credits** | **Internal marks** | **End Term Marks** | **Total** |
| 1 | CC-1 | B-ELE-N101 | Electronic Devices and Circuits-I | 2 | 25 | 25 | 50 |
| B-ELE-N102 | Network Analysis | 2 | 25 | 25 | 50 |
| B-ELE-N103 | Practical -I | 2 | 25 | 25 | 50 |
| 2 | CC-2 | B-ELE-N201 | Electronic Devices and Circuits-II | 2 | 25 | 25 | 50 |
| B-ELE-N202 | Digital Electronics-I | 2 | 25 | 25 | 50 |
| B-ELE-N203 | Practical -II | 2 | 25 | 25 | 50 |
|  |

**Instructions for the Examiners**

1. Syllabus in each Theory Paper in each semester is divided in 4 units.
	* 1. A student is required to attempt 5 questions in all.
		2. Question No 1 is compulsory, consisting of short answer type questions based on all the 4 units.
		3. Two questions will be set from each unit. A student is required to attempt one question from each unit.
		4. All questions carry equal marks.
2. Use of scientific calculator is permissible.
	* 1. Instructions should be imparted using SI system of units. Familiarity with CGS system of units should also be ensured.
3. Distribution of Marks: 25\*+25\*.

Each theory question paper will be of 25 marks of 3 hours duration and 25 marks in each theory paper are to be awarded through internal assessment in each semester.

1. Work load – two hours per week per theory paper.
2. Practical classes to be conducted during odd as well as even semester.
3. The Practical examination will be held at the end of each semester in one sitting of 3 hours.
4. A candidate is required to perform minimum 6 experiments out of the list provided during course of study in each semester.
5. Distribution of Marks: 25\*+25\*

Each practical examination in each semester will be of 25 marks of 3 hours duration and 25 marks in each practical paper are to be awarded through internal assessment in each semester.

1. Maximum 10 students in one group of practical during course of study and also in examination.

**Note: Each credit equals one hour/week for theory teaching load.**

 **Each credit equals two hours/week for practical teaching load.**

Programme Outcomes (POs) for UG Programme

(Course: Electronics)

|  |  |  |
| --- | --- | --- |
| PO1 | Knowledge | Capable of demonstrating comprehensive disciplinary knowledge gained during course of study |
| PO2 | Communication | Ability to communicate effectively on general and scientific topics with the scientific community and with society at large |
| PO3 | Problem Solving | Capability of applying knowledge to solve scientific and other problems |
| PO4 | Individual and Team Work | Capable to learn and work effectively as an individual, and as a member or leader in diverse teams, in multidisciplinary settings' |
| PO5 | Investigation of Problems | Ability of critical thinking, analytical reasoning and research based knowledge including design of experiments, analysis and interpretation of data to provide conclusions |
| PO6 | Modern Tool usage | Ability to use and learn techniques, skills and modern tools for scientific practices |
| PO7 | Science and Society | Ability to apply reasoning to assess the different issues related to society and the consequent responsibilities relevant to the professional scientific practices |
| PO8 | Life-Long Learning | Aptitude to apply knowledge and skills that are necessary for participating in learning activities throughout the life |
| PO9 | Environment and Sustainability | Ability to design and develop modern systems which are environmentally sensitive and to understand the importance of sustainable development. |
| PO10 | Ethics | Apply ethical principles and professional responsibilities in scientific practices |
| PO11 | Project Management | Ability to demonstrate knowledge and understanding of the scientific principles and apply these to manage projects |

Programme Specific Outcomes (PSOs) for UG Programme
(Course: Electronics)

|  |  |
| --- | --- |
| PSO1 | Students will be able to acquire the basic understanding of the electronic components, principles, working and applications of the electronic devices. |
| PSO2 | Explore technical knowledge in diverse areas of Electronics and experience an environment conducive in cultivating skills for successful career, entrepreneurship and higher studies. |
| PSO3 | Students will acquire experimental skills, research aptitude in the area of electronics that will make them capable of contributing to the academic as well as industrial growth of the country. |

**Semester – I**

**CC-1**

**Paper: B-ELE-N101**

**Electronic Devices and Circuits-I**

**Credits: 2**

**Total Marks: 50**

**Internal Assessment: 25**

**End Term Exam: 25**

**End term examination time: 3 hours**

**Course Objective:** The objectives of teaching this paper are

* + - 1. To make the students familiar with the concepts of physics involved in the working of various electronic devices like PN Diode, Zener Diode and Bipolar Junction Transistor (BJT).
			2. To make the students understand various applications of PN junction Diode and Transistor.

**Course Outcome**: After the end of this paper, the students will be able

1. To understand the physics behind the semiconductors.
2. To understand the construction, working & applications of various semiconductor diodes and transistors.
3. To understand various configurations of transistor and their equivalent circuits.

**Mapping of Course Outcomes to Program Outcomes:**

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***CO’s*** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PSO1** | **PSO2** | **PSO3** |
| **CO1** | 3  | 3 | 2 | 3  | 2 | - |  3  | --  | 2 | 2 | 3 | 3 | 3 | 2 |
| **CO2** | 3  | 3 | 3 | 3 | 3  | 3  |  3  | --  | --  | 2 | 3  | 3 | 3 | 2 |
| **CO3** | 3 | 3 | 3 | 3 | 3  | 3  |  3  | 2 | 2 | 2 | 3  | 3 | 3 | 2 |

 **Unit –I**

**Introduction to Semiconductors**: - Intrinsic and Extrinsic semiconductors, Energy Band diagram, drift and diffusion currents in semiconductors (Basic idea only), Junction diode and its characteristics, Space charge capacitance and diffusion capacitance (Basic idea only), Zener diode, Voltage Regulation using Zener Diode , shunt and series clipping circuit, clamping circuit.

**Unit-II**

**Rectifiers:** - HWR, FWR, Bridge FWR, calculation of rectifier parameters.

Filter circuits: L, C, LC (Calculation of ripple factor for capacitor filter only), Voltage multiplier Circuit.

# Unit –III

**Bipolar Junction Transistor: -** Potential curves in unbiased and biased transistor, Transistor current components, Early effect, Static Characteristics of CB & CE configuration, active, cut off and saturation regions. Transistor current gains (Alpha, Beta, and Gama)

**Unit-IV**

**Transistor Model: -** Transistor as an Amplifier, Ebers-moll model of transistor, Hybrid-Model of transistor, Emitter follower, calculation of transistor amplifier parameters using h-model, comparison of transistor amplifier configuration, Millers – theorem and its dual

**Reference Books:**

1. Integrated Electronics by Millman and Halkias.

2. Basic Electronics and Linear Circuits by NN Bhargava, DC Kulshreshtha (TTTI)

3. Electronics Devices and Circuit by Allen Mottershead

**Semester – I**

**CC-1**

**Paper: B-ELE-N102**

**Network Analysis**

**Credits: 2**

**Total Marks: 50**

**Internal Assessment: 25**

**End Term Exam: 25**

**End term examination time: 3 hours**

**Course Objective:** The objective of teaching this paper is to make

1. the students familiar with various network theorems
2. the students familiar with Two-Port Networks

**Course Outcome**: After the end of this paper, the students will be able to

1. Understanding and apply Mesh and Nodal analysis in electronic circuits.
2. Understand different network theorems and their applications in analyzing electronic circuits.
3. Understand different types of two-port networks and parameters. Also they will be able to analyze their performance.

**Mapping of Course Outcomes to Program Outcomes:**

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***CO’s*** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PSO1** | **PSO2** | **PSO3** |
| **CO1** | 3  | 3 | 2  | 3  | 3 | 3 |  3  | --  | --  | --  | 3 | 3 | 3 | 2 |
| **CO2** | 3  | 3 | 2  | 3 | 3  | 3  |  3  | --  | --  | --  | 3  | 3 | 3 | 2 |
| **CO3** | 3 | 3 | 2  | 3 | 3  | 3  |  3  | --  | --  | --  | 3  | 3 | 3 | 2 |

**Unit-I**

**Network Theorems-I: -**Concept of voltage and current sources, Kirchoff’s Voltage Law, Kirchoff’s Current Law, Mesh Analysis, Nodal Analysis, Source Transformation Technique, Star-Delta Transformation, Superposition Theorem, Examples and problems of each topic.

**Unit-II**

**Network Theorems-II: -**Thevenin’s Theorem, **Norton’s** Theorem, Reciprocity Theorem, Maximum Power Transfer Theorem, Duals and Duality, Millman’s Theorem, examples and problems of each topic.

**Unit –III**

**Two–port Network-I: -**Open Circuit Impedance(Z) Parameters, Short Circuit Admittance (Y) Parameters, Transmission(ABCD) Parameters, Inverse Transmission (A’B’C’D’) Parameters, Hybrid(H) Parameters, Inverse Hybrid(g) Parameters, Inter Relationships of different parameters.

**Unit –IV**

**Two–port Network-II: -**Conversion of Parameters, Dependent sources (CCCS, VCVS, VCCS, CCVS), Inter Connection of Two – Port Networks, T and π Representation, Terminated Two-Port Networks, Lattice Networks, Image Parameters

**Reference Books:**

* + - 1. Circuits and Networks by A. Sudhakar, Shyammohan
			2. Network Analysis, Publication Khanna by G.K. Mithal
			3. Network Analysis, Publication Pearson India by M.E. Van Valkenburg

**Semester – I**

**CC-1**

**Paper: B-ELE- N103**

**Practical-I**

 **Credits: 2**

**Max. Marks: 50**

**Internal Assessment: 25**

**End Term Exam: 25**

**End term examination time: 3 hour (one session)**

**Course Objectives**

The objective of teaching this practical paper is

1. To learn the use of various electronic equipment used for analysis of basic analog circuits.
2. To learn the operation of multimeter, CRO and function generator.
3. To design various circuits on bread board using desecrate components.
4. To learn the functioning of wave shaping circuits.
5. To Analyze and interpret experimental data.

**Course Outcome**

After the end of this paper, the students will be able

1. To operate various equipment used in the design and analysis of basic electronic circuits.
2. To Design electronics circuits based on semiconductor devices and passive components.
3. To present the experimental results and conclusions in the form of written report in clear and concise manner.

**Mapping of Course Outcomes to Program Outcomes:**

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***CO’s*** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PSO1** | **PSO2** | **PSO3** |
| **CO1** | 3  | 3 | 2  | 3  | 3 | 3 |  3  | --  | --  | 2 | 3 | 3 | 3 | 2 |
| **CO2** | 3  | 3 | 2  | 3 | 3  | 3  |  3  | --  | --  | --  | 3  | 3 | 3 | 3 |
| **CO3** | 3 | 3 | 2  | 3 | 3  | 3  |  3  | --  | --  | 3 | 3  | 3 | 3 | 2 |

**Note:** A candidate is required to perform minimum 6 experiments out of the list provided during course of study in this semester.

1. To study the V-I characteristics of PN junction diode.
2. To study the zener diode as voltage regulator.
3. To study half wave voltage multiplier circuits using diode.
4. To study HWR and FWR and measurement of ripple factor with and without C filter.
5. To study diode as clipping .
6. To study diode as clamping element.
7. Study of CB characteristics and calculation of H parameter from graph.
8. Study of CE characteristics and calculation of H parameter from graph.
9. Measurement of voltage, Time period and phase-shift using CRO.
10. Measurement of resistance,L,C value using colour codes and multimeter. Also design and verify the potential divider arrangement using resistances.
11. To verify maximum power transfer theorem for DC network.
12. To study the application of Superposition theorem.
13. To study the application of Thevnin theorem.
14. To study the application of Norton theorem.
15. To study RC circuit as integrating , differentiating circuits and filters.

**Semester – II**

**CC-2**

**Paper: B-ELE- N201**

**Electronic Devices and Circuits –II**

**Credits: 2**

**Total Marks: 50**

**Internal Assessment: 25**

**End Term Exam: 25**

**End term examination time: 3 hours**

**Course Objective:** The objectives of teaching this paper are

To make the students understand the concept of operating point and its stability of a transistor.

 To impart knowledge to students about Multistage Amplifier and its Frequency Response.

To make the students familiar with the working of JFET and MOSFET transistors and their characteristics.

**Course Outcome**: After the end of this paper, the students will be able

1. To bias the transistor properly using a suitable biasing circuit.
2. To understand and analyze the circuits of the Amplifiers.
3. To understand the difference between FET and BJT transistors and their working.

**Mapping of Course Outcomes to Program Outcomes:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***CO’s*** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PSO1** | **PSO2** | **PSO3** |
| **CO1** | 3  | 3 | 2  | 3  | 3 | 3 |  3  | --  | --  | --  | 3 | 3 | 3 | 2 |
| **CO2** | 3  | 3 | 2  | 3 | 3  | 3  |  3  | --  | --  | --  | 3  | 3 | 3 | 2 |
| **CO3** | 3 | 3 | 2  | 3 | 3  | 3  |  3  | --  | --  | --  | 3  | 3 | 3 | 2 |

**Unit-I**

**Transistor Biasing Techniques-I: -**Why Bias a Transistor, Selection of Operating Point, need for Bias Stabilization, Requirement of a Biasing Circuit, Different Biasing Circuits: Fixed-Bias Circuit, Collector-to-base Bias Circuit.

**Unit-II**

**Transistor Biasing Techniques-II: -** Bias Circuit with Emitter Resistor, Voltage Divider Biasing Circuit, Emitter-Bias Circuit, Bias Compensation, Thermistor and sensistor Compensation, Thermal Runaway, Frequency response of an amplifier.

**Unit-III**

**Coupling Techniques: -** How to couple two stages, Resistance-Capacitance Coupling, Transformer Coupling, Direct Coupling, Frequency Response Curve of an RC-Coupled CE Amplifier of two stage: Fall of Gain in Low-frequency Range, fall in gain of high Frequencies, Bandwidth of an amplifier, Gain of a multi-stage amplifier.

**Unit-IV**

**Field Effect Transistor: -** Junctions Field Effect Transistor, Qualitative Description of JFET, Drain and transfer characteristics of JFET, FET small signal low frequency model, CS & CD low frequency model, MOSFET -Depletion and enhancement and their drain & transfer characteristics, CMOS (Basic idea).

**Reference Books:**

1. Basic Electronics and Linear Circuits by NN Bhargava, D C Kulshreshtha.
2. Integrated Electronics by Millman and Halkian.
3. Electronics Devices and Circuit by Allen Mottershead.

**Semester – II**

**CC-2**

**Paper: B-ELE-N202**

**Digital Electronics-I**

**Credits: 2**

**Total Marks: 50**

**Internal Assessment: 25**

**End Term Exam: 25**

**End term examination time: 3 hours**

**Course Objective:** The objectives of teaching this paper are

1. To make the students familiar with various number systems and their inter-conversion.
2. To acquaint the students with basic logic gates, Boolean algebra and hardware minimization techniques used while designing digital circuits.
3. To impart knowledge to students about various logic families and arithmetic combinational circuits.

**Course Outcome**: After the end of this paper, the students will be able

1. To convert a number from one system to another number system.
2. To design a digital circuit with optimized hardware required.
3. To understand various logic families and combinational circuits.

**Mapping of Course Outcomes to Program Outcomes:**

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***CO’s*** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PSO1** | **PSO2** | **PSO3** |
| **CO1** | 3  | 3 | 2  | 3  | 3 | 3 |  3  | --  | --  | --  | 3 | 3 | 3 | 2 |
| **CO2** | 3  | 3 | 2  | 3 | 3  | 3  |  3  | --  | --  | --  | 3  | 3 | 3 | 2 |
| **CO3** | 3 | 3 | 2  | 3 | 3  | 3  |  3  | --  | --  | --  | 3  | 3 | 3 | 2 |

**Unit-I**

**Number Systems:** - Binary, Octal, Hexadecimal number system and base conversions, Binary Arithmetic operations, 1’s and 2’s complement representation and their arithmetic, Binary codes-BCD, Grey, cyclic, Error detecting and correcting codes, ASCII, EBCDIC, BCD addition.

**Unit-II**

**Logic Gates and Boolean Algebra: -**Logic Level: Positive and Negative logic level, Logic Gates: AND, OR, NOT, XOR, XNOR, NOR, NAND (Definition, Symbols& Truth table).

Boolean Algebra: Postulates, Duality Principle, De Morgan’s Law, Simplification of Boolean Identities, Standard SOP & POS Forms, Simplification using K-map (upto 4 variables), don’t care condition, implementation of SOP & POS form using NAND and NOR Gate.

**Unit III**

**Logic families: -** Unipolar & Bipolar Logic families, characteristics of Digital IC’s (fan in, fan out, propagation delay. Noise Margin, level of Gating), RTL (NOR), DTL (NAND),TTL (NAND), CMOS Logic gate (NAND, NOR).

**Unit-IV**

**Combinational Circuits:-**Design principle of combinational circuit: Half adder, full adder, half subtractor, full subtractor, Railway track switching system, common light switching for a group of flats, Parity Generator.

**Reference Books:**

1. Digital Electronics by R.P. Jain
2. Digital Computer Electronics by Aalbert Paul Malvino.

**Semester – II**

**CC-2**

**Paper: B-ELE-N203**

**Practical-II**

 **Credits: 2**

**Max. Marks: 50**

**Internal Assessment: 25**

**End Term Exam: 25**

**End term examination time: 3 hours (one session)**

**Course Objectives**

The objective of teaching this practical paper is

1. To learn the use of various electronic equipment used for analysis of basic analog & digital circuits.
2. To designing various circuits on bread board using discrete components & IC.
3. To Analyze and interpret experimental data.

**Course Outcome**

After the end of this paper, the students will be able

1. To operate various equipment used in the design and analysis of basic analog & digital circuits.
2. To Design electronics circuits based on semiconductor devices and passive components.
3. To present the experimental results and conclusions in the form of written report in clear and concise manner.

**Mapping of Course Outcomes to Program Outcomes:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***CO’s*** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PSO1** | **PSO2** | **PSO3** |
| **CO1** | 3  | 3 | 2  | 3  | 3 | 3 |  3  | --  | --  | 2 | 3 | 3 | 3 | 2 |
| **CO2** | 3  | 3 | 2  | 3 | 3  | 3  |  3  | --  | --  | 2 | 3  | 3 | 3 | 2 |
| **CO3** | 3 | 3 | 2  | 3 | 3  | 3  |  3  | --  | --  | 3 | 3  | 3 | 3 | 3 |

**Note:** A candidate is required to perform minimum 6 experiments out of the list provided during course of study in this semester.

1. Study of fixed bias arrangement for transistors.
2. Study of voltage divider biasing arrangement for transistors.
3. Study of two stage R-C coupled transistor amplifier.
4. Study of JFET characteristics.
5. Design of basis logic gates using discrete components.
6. Study of DTL NAND gate.
7. Study of TTL NAND gate.
8. Digital trainer using AND, OR & NOT gates.
9. Digital trainer using NAND gates.
10. Design a half adder using IC 7400.
11. Design a full adder using two half adders.
12. Study of parity generator/checker.